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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,828	03/31/2000	Yuval Ofek	07072-097001	2351

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EXAMINER

NGUYEN, MIKE

ART UNIT	PAPER NUMBER
	2182

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

7D

Office Action Summary	Application N .	Applicant(s)
	09/540,828	OFEK ET AL.
	Examiner	Art Unit
	Mike Nguyen	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 April 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-56 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 31 March 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>27, 2</u> .	6) <input type="checkbox"/> Other: _____

JB

DETAILED ACTION

1. Applicant's amendment filed on 04/03/2003 in response to Examiner's Office Action has been reviewed. The following rejections now apply.
2. Claims 1-56 are pending for the examination.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-56 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 09/540,825. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious to be grouped "a plurality of first directors" and "a plurality of second directors" into "a plurality of first director boards" and "a plurality of second director boards" in the system interface, or the data storage system in order to provide more reliable in transferring data of system interface and to protest

against total system failure in the event of a failure in a component or subassembly of the storage system. In addition, it would have been obvious to put "a switch" in either the boards or the message network or both in order to provide same motivation as above.

6. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-56 are rejected under 35 U.S.C. 102(b) as being anticipated by Martin et al. (U.S. Pat. No. 5,214,768).

9. As to claim 1, Martin teaches a system interface comprising:

a plurality of first directors (see figure 1 elements 14, 16, 18, 19 and column 5 lines 20-26);

a plurality of second directors (see figure 1 element 48 and column 5 lines 49-58);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors (see figure 2 elements 82, 92 and column 7 lines 25-34 and figure 7 and column 14 lines 4-18);

a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors (see figures 2A, 7 element 88); and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network (see column 7 lines 35-62) to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section (see column 7 lines 63-68 and column 8 lines 1-18).

10. As to claim 2, Martin teaches the system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory (see figure 3 elements 138, 140, 142, 144 and column 10 lines 56-62);
a controller for transferring the messages between the message network and such one of the first directors (see figure 2 elements 40, 88 and column 7 lines 39-62).

11. As to claim 3, Martin teaches the system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory (see figure 8 element 316 and column 15 lines 62-66);
a controller for transferring the messages between the message network and such one of the second directors (see figure 2 elements 40, 88 and column 7 lines 39-62).

12. Claim 4 is of similar scope as claim 3 and is therefore rejected under same rationale.

13. As to claim 5, Martin teaches the system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory (see figure 3 elements 138, 140, 142, 144 and column 10 lines 56-62);

a microprocessor (see figure 3 elements 124, 126, 128); and
a controller coupled to the microprocessor and the data pipe (see figure 2 elements 40, 122) for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory (see column 7 lines 39-62).

14. As to claim 6, Martin teaches the system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory (see figure 8 element 316 and column 15 lines 62-66);
a microprocessor (see figure 3 elements 124, 126, 128); and
a controller coupled to the microprocessor and the data pipe (see figure 2 element 40, 122) for controlling the transfer of the messages between the message network and such one of the second directors (see figure 2 elements 88, 62, 48) and for controlling the data between the input of such one of the second directors and the cache memory (see column 15 lines 44-58).

15. Claim 7 is of similar scope as claim 6 and is therefore rejected under same rationale.

16. Claim 8 is of similar scope as claim and is therefore rejected under same rationale.

Martin also teaches a data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface (see figure 1 elements 12, 44).

17. Claims 9-14 are of similar scope as claims 2-7 and are therefore rejected under same rationale.

18. As to claim 15, Martin teaches a method for operating a data storage system adapted to transfer data between a host computer/server and a bank of disk drives (see figure 1 elements 12, 44), such method comprising:

transferring messages through a message network with the data being transferred between the host computer/server and the bank of disk drives through a cache memory, such message network being independent of the cache memory (see figure 2A element 88 and column 7 lines 53-68 and column 8 lines 1-18).

19. Claim 16 is of similar scope as claim 8 and is therefore rejected under same rationale.

20. Claims 17-23 are of similar scope as claims 1-7 and are therefore rejected under same rationale.

21. As claim to 24, Martin teaches the system interface recited in claim 1 wherein the messaging network comprises a switch network having a plurality ports, each one of the ports being coupled to corresponding one of the plurality of first and second directors (see figures 2A, 8 element 88 and column 7 lines 35-62 and column 14 lines 56-68 and column 15 lines 1-15).

22. As to claim 25, Martin teaches a system interface comprising:

a plurality of first directors (see figure 1 elements 14, 16, 18, 19 and column 5 lines 20-26);

a plurality of second directors (see figure 1 element 48 and column 5 lines 49-58);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors (see figure 2 elements 82, 92 and column 7 lines 25-34 and figure 7 and column 14 lines 4-18);

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to corresponding one of the plurality of first directors and second directors, such message network being operative independently of the data transfer (see figures 2A, 8 element 88 and column 7 lines 35-62 and column 14 lines 56-68 and column 15 lines 1-15); and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network (see column 7 lines 35-62) to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section (see column 7 lines 63-68 and column 8 lines 1-18).

23. As to claim 26, Martin teaches a system interface comprising:

a plurality of first directors (see figure 1 elements 14, 16, 18, 19 and column 5 lines 20-26);

a plurality of second directors (see figure 1 element 48 and column 5 lines 49-58);
a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors (see figure 2 elements 82, 92 and column 7 lines 25-34 and figure 7 and column 14 lines 4-18);

a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network with such messages by-passing the data transfer and

with such data transfer comprising passing data through the directors to the cache memory in the data transfer section (see column 7 lines 35-68 and column 8 lines 1-18).

24. As claim 27, Martin teaches the system interface recited in claim 26 wherein the message network comprises a switch network having a plurality of ports, each one of the ports being coupled to corresponding one of the plurality of first directors and second directors (see figures 2A, 8 element 88 and column 7 lines 35-62 and column 14 lines 56-68 and column 15 lines 1-15).

25. Claims 28-29 are of similar scope as claims 26-27 and are therefore rejected under same rationale.

26. Claim 30 is of similar scope as claim 25 and is therefore rejected under same rationale.

27. As claim 31, Martin teaches a system interface comprising:

a plurality of directors (see figure 1 elements 14, 16, 18, 19, 48 and column 5 lines 20-26, 49-58);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors (see figure 2 elements 82, 92 and column 7 lines 25-34 and figure 7 and column 14 lines 4-18);

a message network, operative independently of the data transfer section, coupled to the plurality of directors (see figures 2A, 7 element 88); and

wherein the directors control data transfer in response to messages passing between the directors through the messaging network (see column 7 lines 35-62) with such data passing through the cache memory in the data transfer section (see column 7 lines 63-68 and column 8 lines 1-18).

28. As to claim 32, Martin teaches the system interface recited in claim 31 wherein each one of the directors includes:

a data pipe coupled between an input of such one of the directors and the cache memory (see figure 3 elements 138, 140, 142, 144 and column 10 lines 56-62 and figure 8 element 316 and column 15 lines 62-66); and

a controller for transferring the messages between the message network and such one of the directors (see figure 2 elements 40, 88 and column 7 lines 39-62).

29. As to claim 33, Martin teaches the system interface recited in claim 31 wherein the messaging network comprises a switch network having a plurality of ports, each one of the ports being coupled to corresponding one of the plurality of first directors and second directors (see figures 2A, 8 element 88 and column 7 lines 35-62 and column 14 lines 56-68 and column 15 lines 1-15).

30. Claim 34 is of similar scope as claim 32 and is therefore rejected under same rationale.

31. Claim 35 is of similar scope as claim 31 and is therefore rejected under same rationale.

Martin also teaches a data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface (see figure 1 elements 12, 44).

32. Claims 36-38 are of similar scope as claims 32-34 and are therefore rejected under same rationale.

33. Claims 39-42 are of similar scope as claims 31-34 and are therefore rejected under same rationale.

34. As to claim 43, Martin teaches a system interface comprising:

a plurality of directors (see figure 1 elements 14, 16, 18, 19, 48 and column 5 lines 20-26, 49-58);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors (see figure 2 elements 82, 92 and column 7 lines 25-34 and figure 7 and column 14 lines 4-18);

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to corresponding one of the plurality of directors, such message network being operative independently of the data transfer (see figures 2A, 8 element 88 and column 7 lines 35-62 and column 14 lines 56-68 and column 15 lines 1-15); and

wherein the directors control data transfer in response to messages passing between the directors through the messaging network with such data passing through the cache memory in the data transfer section (see column 7 lines 35-68 and column 8 lines 1-18).

35. As to claim 44, Martin teaches a system interface comprising:

a plurality of directors (see figure 1 elements 14, 16, 18, 19, 48 and column 5 lines 20-26, 49-58);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of directors (see figure 2 elements 82, 92 and column 7 lines 25-34 and figure 7 and column 14 lines 4-18);

a message network, operative independently of the data transfer section (see figures 2A, 7 element 88); and

wherein the directors control data transfer in response to messages passing between the directors through the messaging network with such messages by-passing the data transfer section

and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section (see column 7 lines 35-68 and column 8 lines 1-18).

36. Claim 45 is of similar scope as claim 33 and is therefore rejected under same rationale.
37. Claims 46-47 are of similar scope as claims 44-45 and are therefore rejected under same rationale.
38. Claim 48 is of similar scope as claim 43 and is therefore rejected under same rationale.
39. Claims 49-52 are of similar scope as claims 31-34 and are therefore rejected under same rationale.
40. Claim 53 is of similar scope as claim 31 and is therefore rejected under same rationale.

Martin also teaches a data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface (see figure 1 elements 12, 44).

41. Claims 54-56 are of similar scope as claims 32-34 and are therefore rejected under same rationale.

Response to Arguments

42. In response to the applicant's arguments that Martin does not teach: the messages pass through the message network. In figures 2, 7 element 88 and column 7 lines 39-62 and column 14 lines 56-68 and column 15 lines 1-16, it indicates that the message network 88 provides the central point for distributing control information (messages) in the system interface.

Rebuttal

43. Applicant's look of argument to the Double Patent rejection in the 11/06/2002 Office Action is construed to be acquiescence to the Examiner position.

Conclusion

44. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

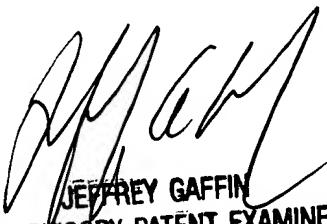
45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 746-7240.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 308-3301.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

Mike Nguyen
Patent Examiner
Group Art Unit 2182
06/11/2003



JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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